PHILOSOPHICAL TRANSACTIONS OF THE ROYAL SOCIETY A MATHEMATICAL, PHYSICAL & ENGINEERING SCIENCES

Microtechnology

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Phil. Trans. R. Soc. Lond. A 1978 **289**, 93-101
doi: 10.1098/rsta.1978.0048

Phil. Trans. R. Soc. Lond. A. **289**, 93–101 (1978)
Printed in Great Britain

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The ability of the semiconductor industry to fabricate complex electronic circuits containing, say, 10000 components in a single crystal of silicon of dimensions 5 mm × 5 mm × 0.2 mm has become almost a commonplace, as the basis for semiconductor memories, microprocessors, calculators, electronic watches, etc. It has led to the concept of 'the pervasiveness of silicon technology'.

The purpose of this paper is to discuss how and why this technology has developed to date, and to consider the ways in which past trends are likely to continue in the next decade. In particular it suggests ways in which the skills of the telecommunications system designer and of the silicon process engineer need to be brought more closely together in the future in order to ensure that the telecommunications industry is able to make optimum use of this dominant field of electronic technology – the silicon integrated circuit.

1. Introduction

By microtechnology I mean the technology of the integrated circuit. In the late 1950s, only a decade after the development of the transistor, it was recognized that within the same single crystal chip of silicon it should be possible to fabricate not only a modest number of transistors and diodes, but also the other key electronic components, resistors and capacitors. This concept was initially termed the silicon solid circuit and later the silicon integrated circuit (s.i.c.). In the past two decades the technology has developed to the point where s.i.cs containing approximately 100000 active components are commercially available. Such s.i.cs consist of a single crystal chip of silicon, typically 5 × 5 × 0.25 mm in size, mounted in a package of typical dimensions 2 × 1 × 0.5 cm, from which the one 'micro' aspect of this technology is self-evident.

Indeed the original incentive to develop this technology stemmed from the twin needs of reducing the size of electronic equipment while simultaneously increasing both its complexity and its reliability.

After one or two false starts using alternative technological approaches, the electronics industry, or more specifically the semiconductor industry, homed in on the use of silicon technology as the way to improve simultaneously the size, reliability and complexity/sophistication of electronics equipment.

At this stage nothing has been said about two key parameters, cost and performance. In fact, however, what has happened is that the changes in technology and design which were introduced in the interest of size reduction and reliability improvement, have *ipso facto* led to dramatic reductions in cost and improvement in performance. It is the cost reduction in particular which has led to the much publicized concept of the pervasiveness of silicon technology, the point being not simply the increased penetration of silicon integrated circuits in the electronic industry, but also both their use in rôles previously served by mechanical or electromechanical products (e.g. watches and telecommunications switching) and in totally

new applications which were not previously economically practicable (e.g. pocket calculators and sophisticated telephone handsets).

It is against this background that the purpose of this paper is:

(i) to consider progress to date, in terms of cost and performance;

(ii) to discuss some of the implications of this progress in the area of digital systems design;

(iii) to consider the future progress of this technology over the next decade;

(iv) to consider the ways in which telecommunications can best exploit this technology.

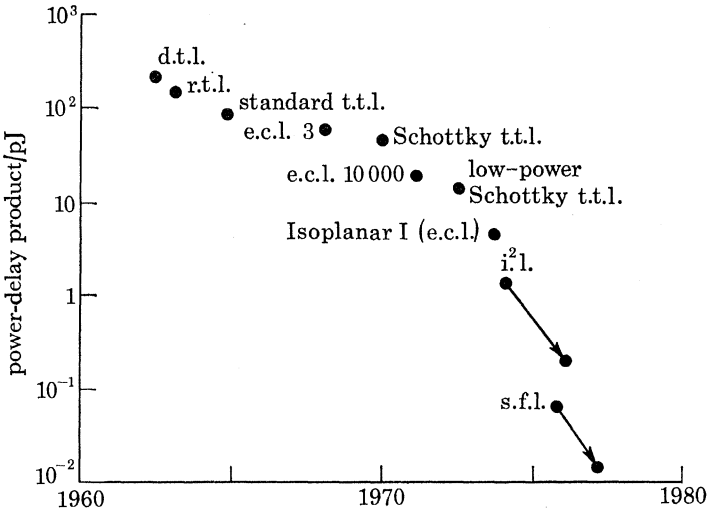

FIGURE 1. A plot of power-delay product against time.

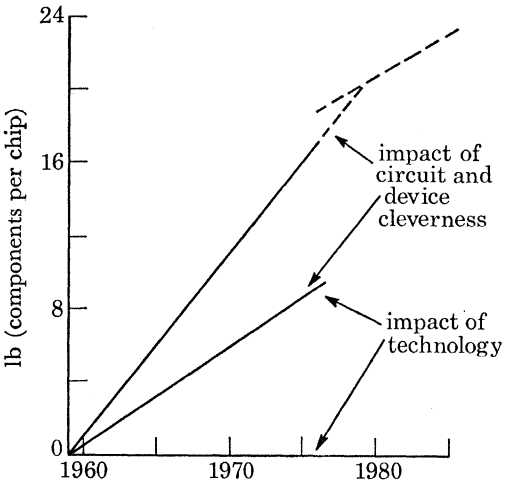

FIGURE 2. A plot of complexity against time.

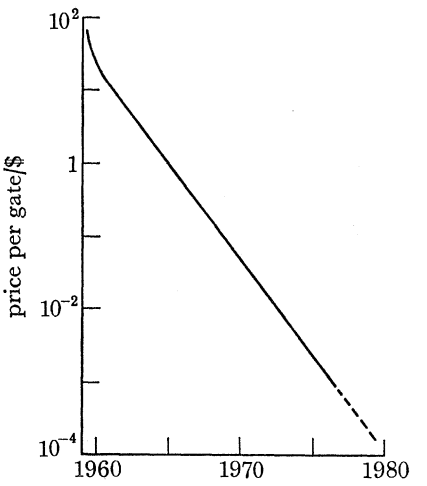

FIGURE 3. A plot of price per gate against time.

2. PROGRESS TO DATE

This can be seen in figures 1–3, which deal respectively with the performance of digital circuits (using power-delay products as the figure of merit), the increased complexity of state-of-the-art products (over the past 15 years), and the subsequent price per logic gate over the same period. A direct result of that progress is the availability at this time of 16 kbit/chip memory products, and microprocessors.

A further implication of this progress has been the proliferation of technology – particularly in terms of m.o.s. processes. This is illustrated in table 1, which shows how the simple expression 'm.o.s.' is an oversimplification of a situation more truly represented by approximately 1000 process choices, this choice having significant potential importance to the equipment builder, in terms of both initial cost and reliability.

TABLE 1. THE PROLIFERATION OF M.O.S. PROCESSES

crystal orientation	channel type	mode of operation	gate electrode	gate dielectric	source and drain	substrate
(111)	p	normally off	Al	SiO_2	diffused	bulk
	n	normally on	poly-Si	Si_3N_4	c.c.d.	epitaxial
(100)	p and n	memory	Mo, W, etc.	Al_2O_3	implanted	insulator

number of combinations = 1458.

The current state of the art in complexity terms can be seen in figure 2. In terms of various performance criteria it can be represented by such examples as:

(i) Power delay product: values below 0.1 pJ are achievable with gate delays of a few tens of nanoseconds.

(ii) Gate delay: on-chip gate delays of better than 0.25 ns are achievable.

(iii) Counter input frequency: divide by four circuits operating with inputs above 2 GHz have been made.

(iv) Wideband amplifiers: amplifiers with useful flat gain up to 1 GHz are now available.

(v) Power and voltage: these tend to be chip area/cost limited. Current performance is at the 10–20 W and 100 V level.

(vi) Memory retention: optimized E.A.R.O.M. circuits should give 10 year memory retention.

While in terms of device complexity there would appear to be two orders of magnitude available for extension in the next few years, in the case of performance the available 'stretch factor' would appear to be more like a factor of 2. There appear to be two reasons for this:

(*a*) The fact that basic limitations, such as carrier velocity, are becoming significant.

(*b*) The fact that alternative materials/techniques offer a competitive solution to the same system need. This will be enlarged upon below.

3. THE IMPLICATIONS FOR DIGITAL SYSTEMS DESIGN

These start with a full appreciation of the cost impact of s.i.c. technology. The cost of an s.i.c. is a function of the design/development cost, amortized over the production volume, the manufacturer's efficiency in processing silicon, and in assembling and testing the finished product. The precise relation is given in equation (1):

$$C_N = D + c + N S/n + N (P + A + T), \tag{1}$$

where C_N is the cost of N devices; D the cost of design; c, special capital; S, silicon slice processing; n, good chips per slice; P, package; A, assembly operation; and T, test operation. Further examination of that relation shows that simple s.i.cs are cost-dominated by package, assembly and testing costs, while the cost of complex s.i.cs is determined primarily by silicon

processing (the percentage yield of 'good' product being the dominant factor), and design. This leads to the curve given in figure 4, from which can be identified a broad minimum, toward the optimum scale of integration (o.s.i.), which represents that level of chip complexity which leads to minimum full-time equipment costs.

As is to be expected from the trends illustrated in figure 2, o.s.i. is dramatically time-dependent, leading to the curves shown in figure 5.

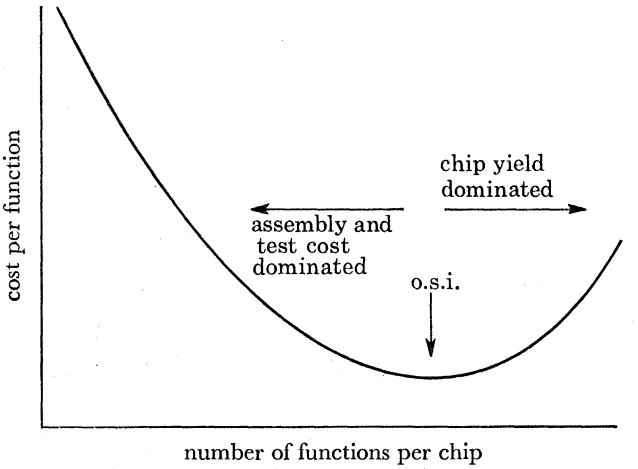

FIGURE 4. A plot of cost against complexity: the optimum scale of integration (o.s.i.).

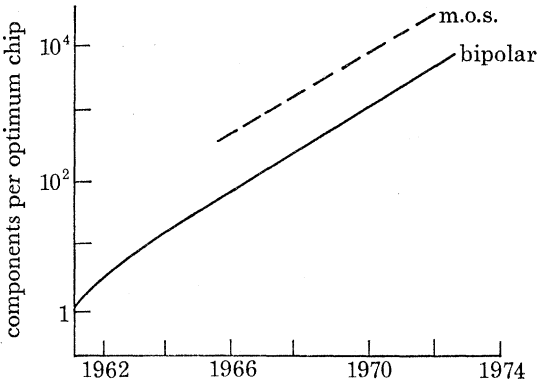

FIGURE 5. A plot of o.s.i. against time.

We thus have a situation where, if the most cost-effective equipment/systems are to be made, then an integrated design/decision process is needed in which silicon is seen as the constructional material for modern electronics, and hence for telecommunications. This optimized integrated decision process can only be achieved by bringing together the full range of expertise which is needed in order to turn silicon crystal into a cost-effective communications network.

Cost optimization is only one of the reasons for this. Other major factors which need to be taken fully into account in designing electronic systems include reliability and s.i.c. performance.

Reliability

The fact that this was one of the early motivators in the development of s.i.c. technology should not lead to the automatic assumption that further increases in chip complexity can

be achieved indefinitely without the creation of new reliability hazards. The concept of an optimum scale of integration for system reliability is illustrated in figure 6. The factors involved in this particular optimization include design integrity, testability, and equipment practice/thermal engineering, in addition to the various silicon technology related factors. It is thus evident that an integrated analysis must be made to maximize reliability, as well as to minimize prime cost.

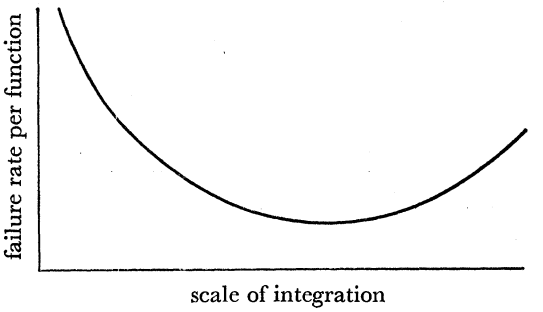

FIGURE 6. O.s.i. for reliability: there is a need to optimize process choice for maximum reliability. The trade-off is in terms of temperature, surface sensitivity, electromigration, assembly/package faults and design sensitivity.

S.i.c. performance

The natural development of s.i.c. technology leads to the availability of new combinations of function, cost and performance which need to be taken into account in system design. It is only too easy for a system designer to base tomorrow's system on yesterday's technology. Since the time scale for the implementation and exploitation of such decisions in the field of telecommunications is particularly long, it is essential that the initial decisions should be close to optimal. This can only be achieved as a result of the same close-knit analysis of problem and options which has already been referred to.

The present level of technological capability offered by the s.i.c. industry already presents telecommunications designers with a variety of product/technology/system choice which is possibly unwelcome and certainly difficult to contain. In fact, though, there is more yet to come.

TABLE 2. V.L.S.I. TARGETS: 1980

bipolar logic	10^5 gates per chip; 10 ns
bipolar logic – high speed	2×10^3 gates per chip; 0.3 ns
bipolar memory	16 kbits per chip; 10 ns
n-m.o.s. memory – dynamic	2×10^6 bytes per wafer; 150 ns

4. FUTURE DEVELOPMENTS IN I.C. TECHNOLOGY

Apart from simply extrapolating the historical data in figures 1 and 2, it is interesting to note some of the objectives of the Japanese Industrial Programme on v.l.s.i. (very large scale integration), as given in table 2. These targets are impressive, not least because they are motivated by the need for system competitiveness rather than by the narrower interests of a semiconductor company. They do, however, leave unanswered certain questions, such as:

(i) What are the physical limitations to these projected increases in complexity and performance?

(ii) How will such complex devices be designed and tested economically?
(iii) How will this complexity capability be applied?
(iv) What are the reliability implications of these continuing complexity trends?
Let us now consider these questions in turn.

4.1. *Limitations*

Various factors which in the limit must impact on the capability of the semiconductor industry to keep on increasing die size, packing density and device performance include:

(*a*) Silicon quality – and, indeed, the quality of other key materials used in processing, such as photo resists.

(***b***) Physical factors such as the wavelength of light, the statistics of impurity distribution, and the basic electronic properties of silicon. Of these, the first to become dominant is the wavelength of light, which when used for exposing photo resist sets a limit to features which can be developed reproducibly at about 2 μm. This explains the current major effort being devoted to the development of electron beam technology both for the production of high quality masks and also for direct device fabrication. It is clear that such technology will become increasingly important in the next few years.

(*c*) Improved production equipment, capable of handling the combination of large slices and smaller device geometrics, while reducing the level of yield-limiting defects introduced during processing.

(*d*) Process simplification, understanding, and control: it seems clear that there must emerge a greater depth of understanding of the impact of each process step on device yield, so that efforts can be concentrated upon improving the control of key process steps. If significant progress is to be made in these directions, the semiconductor industry will have to exercise greater self-discipline and avoid the pitfalls which are generated, particularly in m.o.s. technology, by the cascade development of so many process variants that none are optimized or understood adequately by designer, processor or customer, as illustrated in table 1.

4.2. *Economic design and test*

Even in the case of 'regular' arrays such as r.a.ms, it is clear that the moves from 1 to 4 to 16 k devices have added tremendously to the problems of optimized design and low cost but high security testing. In custom/random logic the situation is more difficult, and it must be recognized by the semiconductor industry that if suitable markets are to be developed at levels approaching, say, one million components per chip, then not only will improved techniques for logic simulation/computer aided layout/circuit simulation and automatic testing be absolutely essential, *but* the ease of achieving such techniques should be a key objective in technology/process development. The point is that design methodology and process innovation should proceed hand in hand if optimal use is to be made of new high packing density processes.

One way of apparently by-passing the design problem is to use microprocessors, and certainly such programmable structures are, with memories, the obvious exploiters of v.l.s.i. However, while microprocessors are clearly a very significant factor in the development of electronics, it would be wrong to assume that they are the appropriate solution to every problem.

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4.3. *Application of process complexity*

Left to itself the semiconductor industry will apply its new capabilities to the generation of 'standard products' which it can sell to the widest possible range of customers. This explains the current major emphasis on microprocessors and memories, these being the class of products which most readily meet the conflicting needs of complexity exploitation and wide customer appeal.

Certainly the emergence of complex/low cost semiconductor memories is of profound significance, as this is what has given reality to the concept of the distribution of processing/intelligence: a concept which is really based on the facility to distribute memory economically.

However, it would be quite wrong for a major systems industry such as telecommunications to assume automatically that its future switching hardware should consist primarily of standard microprocessors and memories. Such *may* indeed be the best solution, but it should be arrived at by having carried out a continuing atoms-to-systems analysis, not by simply and passively responding to the blandishments of the semiconductor industry.

4.4. *Reliability implications*

This has already been considered above, and in figure 6. Increased emphasis on this problem will be essential if the full benefits of the s.i.c. technology are to be achieved at the user-level.

4.5. *Other materials and devices*

Materials other than silicon coupled to new device concepts, are beginning to offer systems designers new degrees of freedom. Examples of such are:

Gallium arsenide

The development of the gallium arsenide J-f.e.t., and more recently of monolithic circuit technology based on that as the key active device, shows every sign of yielding i.cs capable of performing both analogue and digital functions usefully into the 10 GHz frequency range.

Magnetic bubbles

Classically, digital systems engineers have placed high reliance on the availability of low cost serial non-volatile memories. With the development of portable equipment, allied to the concept of distributed intelligence – and memory – there are clearly benefits to be derived from a solid state technology offering high reliability and a flatter 'cost per bit versus size' profile. Magnetic bubbles offer just such a technology.

Surface acoustic wave devices

Apart from developing a useful rôle in their own right in such fields as i.f. filters for colour television sets, high quality oscillators and 'chirp' filters for radar signal processing, it is clear that in some applications the use of analogue signal processing using s.a.w. devices must be compared at the system level with the use of digital techniques based for example on the exploitation of charge coupled devices. These two technologies should not be viewed as competitive, but rather as complimentary, a mode in which they present a significant challenge to the innovative skills of systems designers and device designers working coherently.

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5. Exploitation of s.i.c. technology in telecommunications

5.1. *The past*

In the past the telecommunications industry has exhibited a high degree of vertical integration, which led to two favourable characteristics:

(i) Total design control: the industry was, within itself, able to make the overall decisions on how best to employ copper and steel in the provision of an acceptable telecommunications service.

(ii) Maintenance of added value: this was self-evident in the light of the degree of vertical integration.

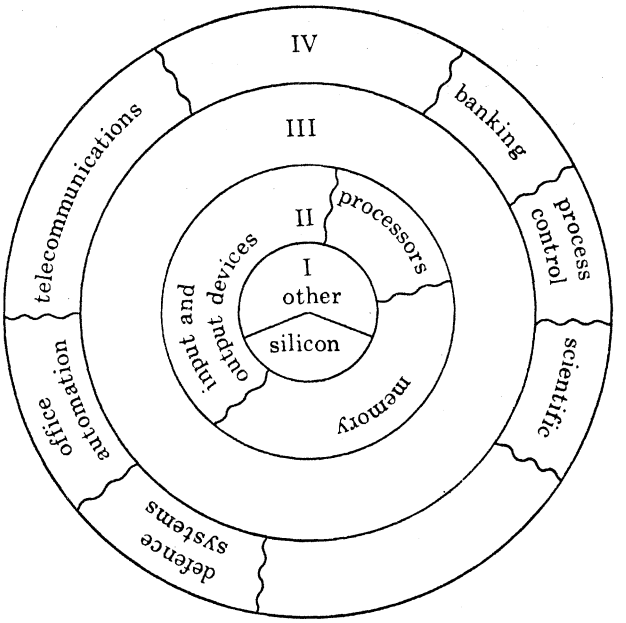

Figure 7. The digital systems industry. Zone I represents technology; II, hardware; III, applications software (couples II and IV); IV, applications.

5.2. *The present*

The telecommunications industry is now faced with a number of new situations: a mixture of problems, threats and opportunities. To highlight just a few, they are as follows:

(*a*) Unless it takes steps to retrieve the situation, it has abandoned both total design control and the maintenance of added value. The purpose of this paper is to advocate that it *should* retrieve the situation.

(*b*) This situation has developed in a period of profound technological change, when making the correct systems/technology decisions would be difficult enough even in a total design control mode.

(*c*) At the same time, this is a period of application/service innovation, in which the degree of overlap with industries such as e.d.p., office equipment, consumer electronics, etc., is also changing rapidly. This leads to a new kind of competitive environment with companies whose reaction time may be closer to the time constants associated with the changes in technology.

(*d*) On the other hand, this period of innovation also presents the telecommunications

industry with a tremendous opportunity to participate in these new markets, and to do so from a position of major strength in system understanding and implementation.

5.3. *The future*

In order to exploit the opportunity referred to in §5.2 (*d*), and at the same time to continue to compete effectively in its traditional areas, it is important that the telecommunications industry should return to the situation referred to as total design control coupled with maintenance of added value. To do this, it must recognize the essential unity of the total process of applying technology in a telecommunications network, as illustrated in figure 7, in which the following points are made:

(*a*) that telecommunications should be viewed as part of a total digital systems industry;

(*b*) that technology is at the core of this industry;

(*c*) that as technology develops, so must the hardware *and* software disciplines in order to adapt these changes in technology to the end-application.

In practice this means that the wide variety of new technology – silicon, microprocessor, memory, optical, microwave, etc. – must be understood in terms of its system design implications and time scale, if the correct system decisions are to be made. Specifically in the case of silicon integrated circuits this means establishing the integrated design capability which can optimize the use of 'standard' and 'user-orientated special' i.cs. Furthermore, it means sufficient design involvement in the latter case to participate in solving the test and reliability problems which were referred to in §§4.2 and 4.4 above.

6. Conclusions

The future growth of telecommunications is closely tied to the present and future growth of solid state electronic technology. Recognition of this close relation, and of the need for an atoms-to-systems design capability will ensure the long term health of the telecommunications industry. Any lack of such recognition, by continuing an 'arms-length' relation with the purveyors of new technology, reduce the future competitiveness of this major industry. The lesson is clear: integration presents both the challenge and the solution.

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